Name: Ningyuan Zhang

Section: A

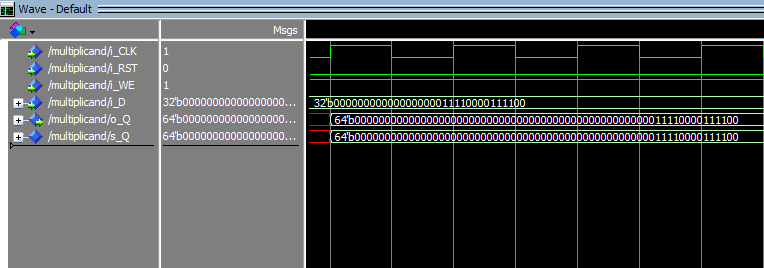
Date: 3/1/2017

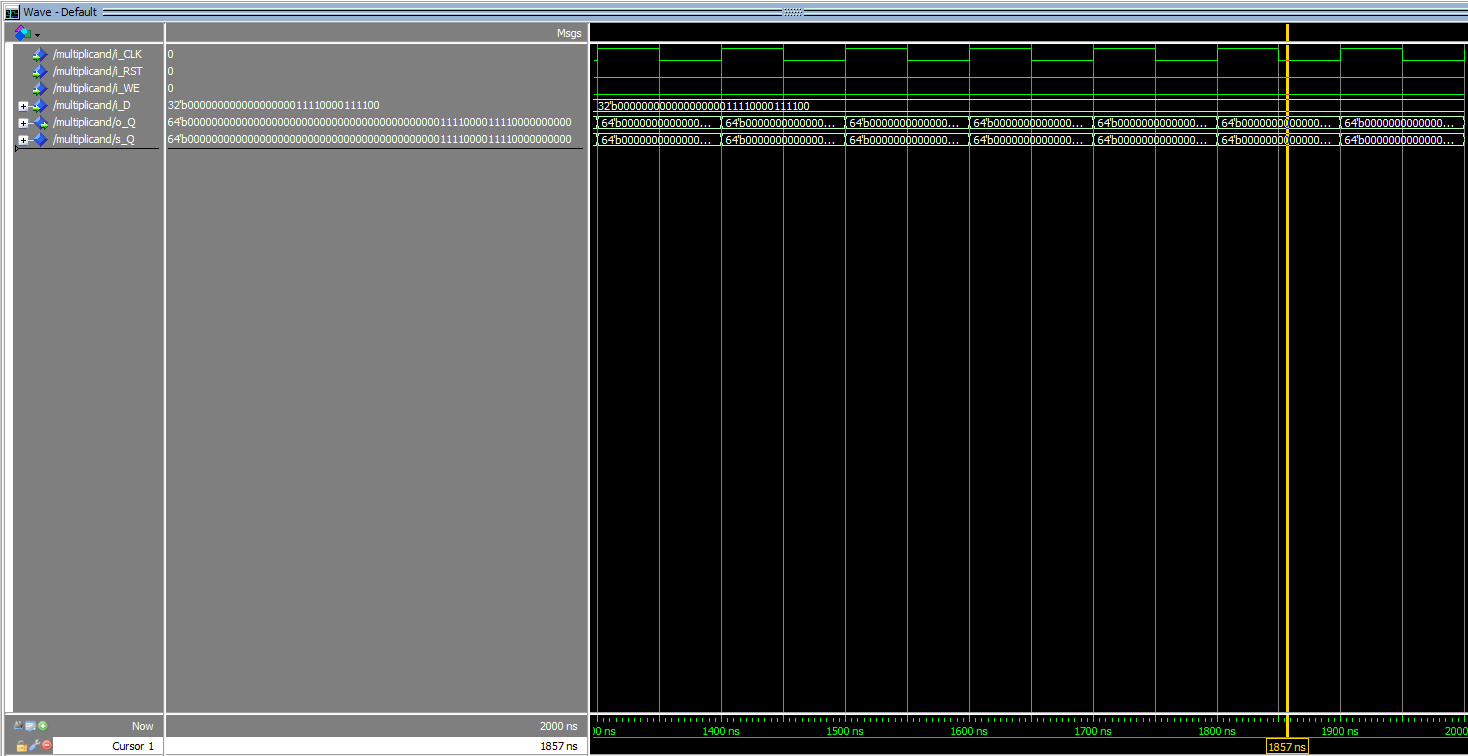
Instructor: Akhilesh Tyagi

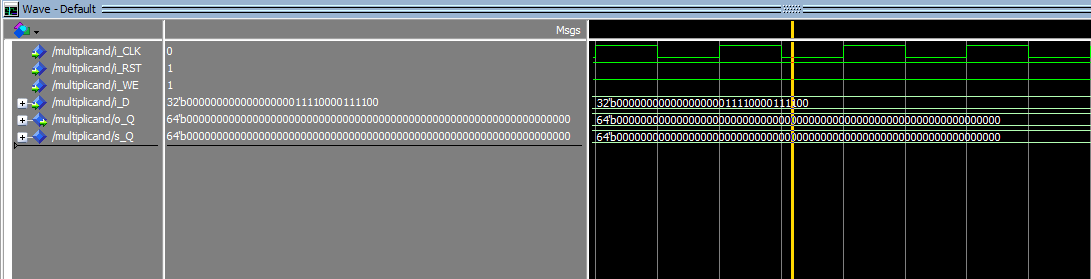
Lab-6

1. **Multiplicand**

the code was contained in file multiplicand.vhd



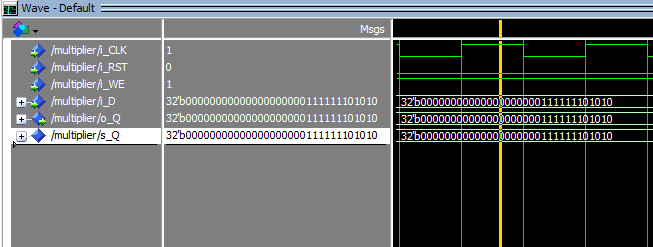


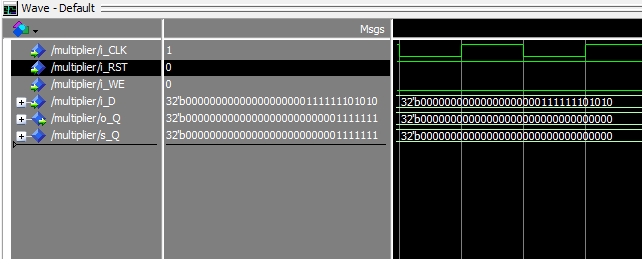
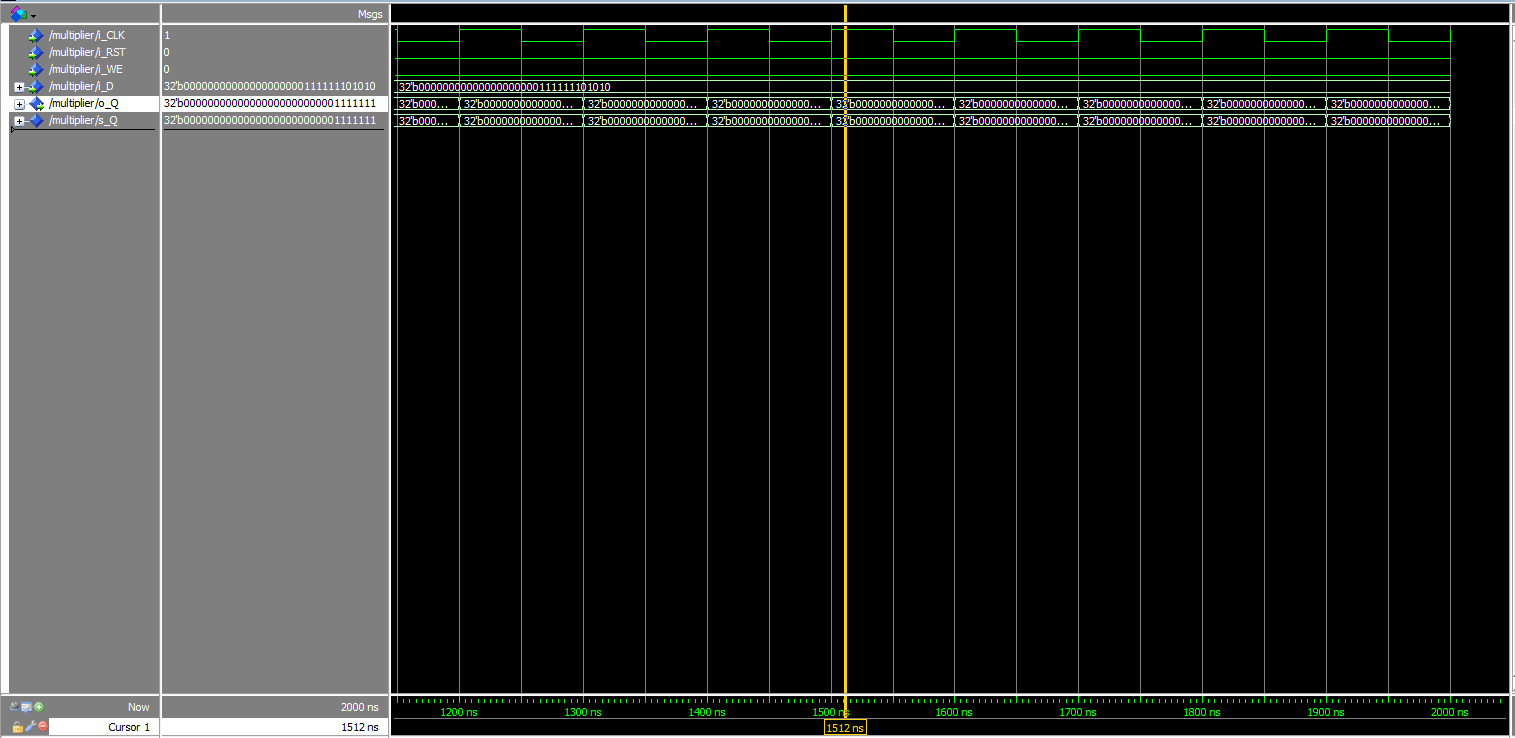


I did not use the instruction sll (shift left logiccally) in my shift motion, instead I directly added 0 into right side and popped out the most left bit.

**2. Multiplier**

the code file was multiplier.vhd



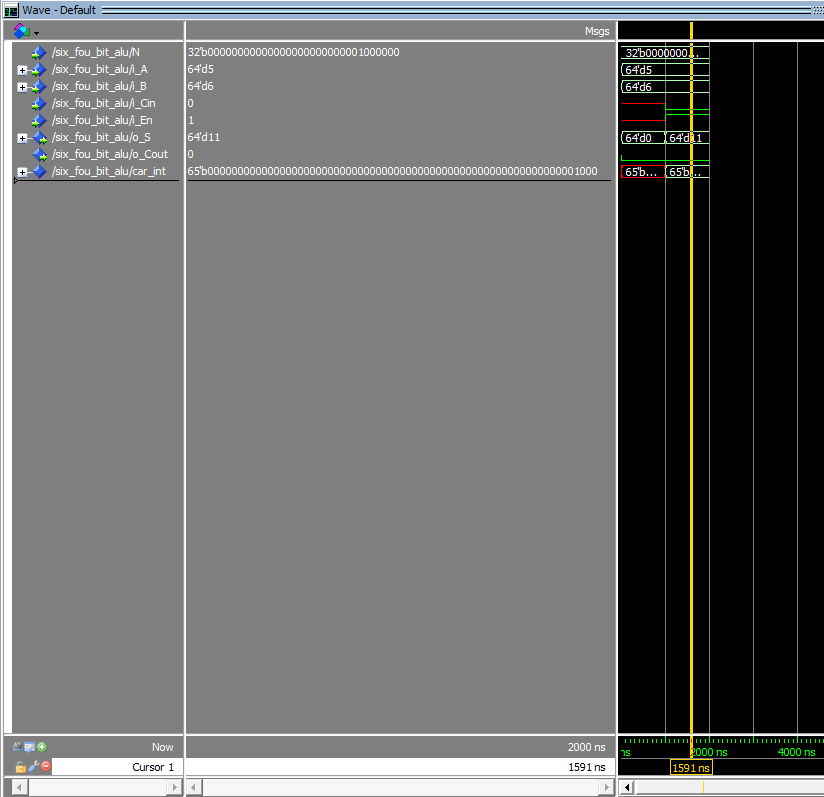


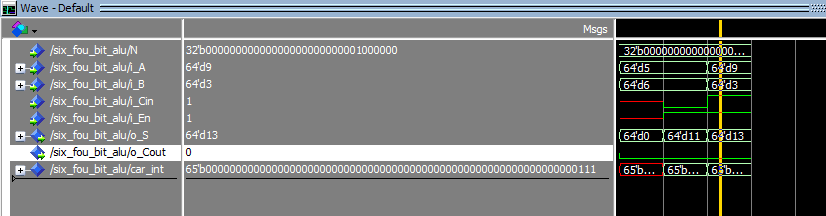
I did not use the instruction srl (shift right logiccally) in my shift motion, instead I directly added 0 into left side and popped out the most right bit.

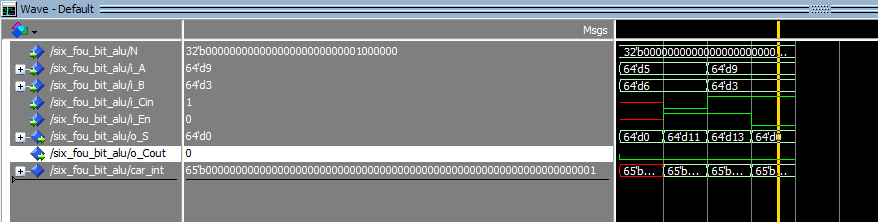
**3. 64-bit ALU**

the code file was six\_fou\_bit\_ALU.vhd

I use VHDL directly to write the file.







**4. Multiplication**

the 64-bit two to one mux file was six\_fou\_ttomux.vhd

and the 64-bit register was six\_fou\_single\_reg.vhd

the final multiplication called lab6.vhd

